



Figure 1. Flowchart of declared system

Figure 2

P_1	P_2	P_3
P_8	P	P_4
P_7	P_6	P_5

[illegible]

Figure 3

dir order	0	1	2	3	4	5	6
0	(-3,0)	(-2,0)	(-1,0)	(0,0)	(1,0)	(2,0)	(3,0)
1	(-3,-1)	(-2,0)	(-1,0)	(0,0)	(1,0)	(2,0)	(3,1)
2	(-3,-1)	(-2,-1)	(-1,0)	(0,0)	(1,0)	(2,1)	(3,1)
3	(-3,-2)	(-2,-1)	(-1,-1)	(0,0)	(1,1)	(2,1)	(3,2)
4	(-3,-3)	(-2,-2)	(-1,-1)	(0,0)	(1,1)	(2,2)	(3,3)
5	(-2,-3)	(-1,-2)	(-1,-1)	(0,0)	(1,1)	(1,2)	(2,3)
6	(-1,-3)	(-1,-2)	(0,-1)	(0,0)	(0,1)	(1,2)	(1,3)
7	(-1,-3)	(0,-2)	(0,-1)	(0,0)	(0,1)	(0,2)	(1,3)
8	(0,-3)	(0,-2)	(0,-1)	(0,0)	(0,1)	(0,2)	(0,3)
9	(1,-3)	(0,-2)	(0,-1)	(0,0)	(0,1)	(0,2)	(-1,3)
10	(1,-3)	(1,-2)	(0,-1)	(0,0)	(0,1)	(-1,2)	(-1,3)
11	(2,-3)	(1,-2)	(1,-1)	(0,0)	(-1,1)	(-1,2)	(-2,3)
12	(3,-2)	(2,-1)	(1,-1)	(0,0)	(-1,1)	(-2,1)	(-3,2)
13	(3,-1)	(2,-1)	(1,0)	(0,0)	(-1,0)	(-2,1)	(-3,1)
14	(3,-1)	(2,0)	(1,0)	(0,0)	(-1,0)	(-2,0)	(-3,1)
15	(3,0)	(2,0)	(1,0)	(0,0)	(-1,0)	(-2,0)	(-3,0)

Figure 4

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	1	1	0	1	1	0	0	1	1	1	1	0	1	0	0
1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	0	0
2	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
3	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
6	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
7	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
8	1	0	1	0	1	1	1	0	1	1	1	1	1	1	1	0
9	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
A	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
B	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
C	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	0
D	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0
E	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1
F	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1

0 1 2 3 4 5 6 7 8 9 A B C D E F
0 1 1 1 0 1 1 0 0 1 1 1 1 0 1 0 0
1 1 1 1 1 1 1 1 1 0 1 1 1 0 1 0 0
2 1 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1
3 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1
4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
6 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1
7 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1
8 1 0 1 0 1 1 1 0 1 1 1 1 1 1 1 0
9 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0
A 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
B 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
C 0 0 1 0 1 1 1 0 1 1 1 1 1 1 1 0
D 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0
E 0 0 1 0 1 1 1 0 1 1 1 1 1 1 1 1
F 0 0 1 0 1 1 1 0 1 1 1 1 1 1 1 1

Figure 5

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	1	1	0	1	1	0	0	1	1	0	0	0	1	0	0
1	1	1	1	1	1	1	1	1	0	1	0	0	0	1	0	0
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0
8	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
A	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
B	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
C	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1
D	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
E	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
F	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Figure 5 is a truth table for a 16-input, 16-output logic function. The inputs are labeled 0 through F, and the outputs are labeled 0 through F. The table shows the output for each combination of inputs. The output is 1 if the input is 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, or F. The output is 0 if the input is 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, or F.